Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

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1-20. (Cancelled).

21. (Currently amended) A method ~~for setting a data transfer rate for multiple memory modules~~, comprising:

receiving memory module attribute information from attribute memories in each memory module in the multiple memory modules;

receiving memory attachment position information that indicates memory slots to which each of the multiple memory modules is attached;

receiving an upper limit temperature at which each memory module in the multiple memory modules is operated;

individually determining data transfer rates for each memory module in the multiple memory modules based at least in part upon all of the corresponding received memory module attribute information, the received upper limit temperature, and the received attachment position information; and

collectively setting a data transfer rate with respect to the multiple memory modules based at least in part on the individually determined data transfer rates.

22-23. (Cancelled)

24. (Previously presented) The method of claim 21, wherein the data transfer rate set collectively for the multiple memory modules is an upper limit value of a data transfer rate at which

a host controller accesses one of the multiple memory modules relative to a maximum data transfer rate at which the host controller can access the one of the multiple memory modules.

25. (Currently amended) The method of claim 21, wherein determining data transfer rates individually for each memory module in the multiple memory modules comprises:

accessing a setting value candidate database; ~~and~~

retrieving a candidate data transfer rate from the setting value candidate database for at least one memory module in the multiple memory modules, the candidate data transfer rate from the setting value candidate database is located based at least in part upon memory attribute information stored in the at least one memory module;

determining a current data transferring rate, which is the data transfer rate currently being used to transfer data;

comparing the current and the candidate data transfer rates; and

setting the data transfer rate based on the comparison.

26. (Previously presented) The method of claim 25, wherein determining data transfer rates individually for each memory module in the multiple memory modules further comprises:

retrieving data transfer rates from the setting value candidate database for each memory module in the multiple memory modules, the data transfer rates from the setting value candidate database are located based at least in part upon memory attribute information stored in each of the memory modules, respectively.

27. (Previously presented) The method of claim 21, wherein collectively setting the data transfer rate with respect to the multiple memory modules comprises:

determining a maximum data transfer rate with respect to data transfer rates determined for each memory module;

determining a minimum data transfer rate with respect to data transfer rates determined for each memory module; and

collectively setting the data transfer rate with respect to the multiple memory modules as a value that is between the maximum data transfer rate and the minimum data transfer rate.

28. (Previously presented) The method of claim 21, wherein collectively setting the data transfer rate with respect to the multiple memory modules comprises:

determining a minimum data transfer rate with respect to data transfer rates determined for each memory module; and

using the minimum data transfer rate as the collective data transfer rate for the multiple memory modules.

29. (Previously presented) The method of claim 21, wherein setting a data transfer rate with respect to the multiple memory modules collectively comprises transferring the data transfer rate with respect to the multiple memory modules to a host controller.

30. (Previously presented) The method of claim 21, wherein the attribute information within at least one memory module of the multiple memory modules includes manufacturer identification information that indicates a manufacturer of the at least one memory module, number-of-devices information that indicates a number of devices on the at least one memory module, memory bank information that indicates whether the at least one memory module is of a single-sided or of a double-sided implementation, and type identification information that identifies a type of the at least one memory module.

31. (Currently amended) An apparatus, comprising:

a memory that includes instructions for:

acquiring first memory attribute information for a first memory module from an attribute memory in the first memory module;

acquiring second memory attribute information for a second memory module from an attribute memory in the second memory module, wherein the acquired first memory attribute information and the acquired second memory attribute information include Serial Presence Detect information;

determining a first data transfer rate setting value for the first memory module based at least in part upon the acquired first memory attribute information;

determining a second data transfer rate setting value for the second memory module based at least in part upon the acquired second memory attribute information;

analyzing the first data transfer rate setting value and the second data transfer rate setting value;

determining a data transfer rate setting value that is to be applied to the first memory module and the second memory module based at least in part upon the analysis of the first data transfer setting value and the second data transfer rate setting value; and

storing the data transfer rate setting value that is to be applied to the first memory module and the second memory module; and

a processor that is configured to execute the instructions in memory.

32. (Previously presented) The apparatus of claim 31, wherein the memory comprises further instructions for selecting a data transfer rate setting value that is between the first data transfer rate setting value and the second data transfer rate setting value.

33. (Previously presented) The apparatus of claim 31, wherein the memory comprises further instructions for:

determining which of the first data transfer rate setting value and the second data transfer rate setting value is lower; and

selecting the lower data transfer rate setting value as the data transfer rate setting value that is to be applied to the first memory module and the second memory module.

34. (Previously presented) The apparatus of claim 31, wherein the memory comprises additional instructions for:

acquiring first memory attachment position information that is indicative of a memory slot to which the first memory module is attached;

acquiring second memory attachment position information that is indicative of a memory slot to which the second memory module is attached;

determining the first data transfer rate setting value based at least in part upon the first memory attribute information and the first memory attachment position information; and

determining the second data transfer rate setting value based at least in part upon the second memory attribute information and the second memory attachment position information.

35. (Previously presented) The apparatus of claim 31, wherein the memory comprises additional instructions for:

accessing a setting value candidate database;

using at least a portion of the first memory attribute information as an index with respect to contents of the setting value candidate database to determine the first data transfer rate setting value; and

using at least a portion of the second memory attribute information as an index with respect to contents of the setting value candidate database to determine the second data transfer rate setting value.

36. (Previously presented) The apparatus of claim 31, wherein the memory comprises additional instructions for:

acquiring a first upper limit temperature at which the first memory module is operated externally through a host controller;

acquiring a second upper limit temperature at which the second memory module is operated externally through the host controller;

determining the first data transfer rate setting value based at least in part upon the first upper limit temperature; and

determining the second data transfer rate setting value based at least in part upon the second upper limit temperature.

37. (Currently amended) The apparatus of claim 31, ~~wherein the acquired first memory attribute information and the acquired second memory attribute information include Serial Presence Detect information~~ further including determining the first and second data transfer rate setting values according to a heating value, wherein the heating value is determined in accordance with a total number of memory devices implemented in the memory module, an implementation state of the memory devices, a type of the memory devices, and a manufacturer of the memory devices.

38. (Currently amended) A computer-readable medium comprising computer-executable instructions for:

acquiring memory attribute information for each memory module in a plurality of memory modules, wherein each of the memory modules include an attribute memory that retains the memory attribute information;

accessing a setting value candidate database;

locating candidate data transfer rate setting values for each memory module in the plurality of memory modules in the setting value candidate database, wherein the candidate data transfer rate setting values correspond to the acquired memory attribute information in the setting value candidate database;

obtaining current data transfer rates for the each of the memory modules in the plurality of memory modules, wherein the current data transfer rate is the data transfer rate currently being used to transfer data;

comparing the current and the candidate data transfer rates; and

determining a data transfer rate setting value that is to be applied with respect to each memory module in the plurality of memory modules based at least in part upon the ~~located candidate data transfer rate setting values~~ comparison; and

outputting the selected data transfer rate setting value to a host controller that controls data transfer with respect to the plurality of memory modules.

39. (Previously presented) The computer-readable medium of claim 38 comprising further computer-executable instructions for:

determining which of the located candidate data transfer rate setting value is lowest; and

selecting the lowest candidate data transfer rate setting value as the value to be output to the host controller.

40. (Previously presented) The computer-readable medium of claim 38, further comprising:

acquiring memory position information for each memory module in the plurality of memory modules, wherein the memory position information indicates to which memory slots of an information processing apparatus each of the memory modules is attached; and

locating the candidate data transfer rate setting values for each memory module in the plurality of memory modules in the setting value candidate database, wherein the candidate data

transfer rate setting values correspond to the acquired memory attribute information and the acquired memory position information in the setting value candidate database.